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High-Power, High-Efficiency GaN HEMT Power Amplifiers for 4G Applications

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New GaN HEMT devices allow the design of high power amplifiers with the desired linearity and efficiency for 4G applications such as WiMAX, UMTS and WCDMA

Today's wireless system requirements demand increasing performance from power amplifiers. The higher gain and output power available from today's transistors reduce the number of amplifier stages, and improved efficiency decreases system DC power requirements and generated heat. But at these higher power and efficiency levels, power amplifier linearity needs to meet or exceed the requirements of past systems. Gallium nitride (GaN) HEMT based power transistors offer an ideal technology solution for these amplifiers due to their exceptionally high operating power density. Cree's GaN HEMT devices deliver RF power densities as high as 8 W/mm [1] of gate periphery due to superior thermal properties provided by the silicon carbide substrates on which they are fabricated. This is of considerable advantage when compared with silicon substrates.

This article details three amplifier designs that cover a variety of 4G frequency bands. The first two designs are 2 GHz Doherty amplifiers with capable peak output power of 480 W employing the new CGH21240F or CGH25240F pre-matched GaN HEMT transistors. These transistors offer twice the peak power of previously released transistors, CGH21120F and CGH25120F, from Cree [2]. Doherty amplifiers offer a unique solution for linear amplifiers since the efficiency is maintained at powers backed off from saturation. The third design is a 900 MHz 120 W saturated power design for lower frequency operation using the new CGH09120F broadband (unmatched) transistor. Linearity of all three designs is maintained through the use of digital pre-distortion (DPD).

Parameter	Requirement
Operating Frequency	2.11-2.17 GHz
Modulation Signal	3GPP WCDMA
Output Power (average)	80 watts
Drain Efficiency	50%
DPD corrected ACLR1	–50 dBc

Table 1 · CDPA21480 design targets.

UMTS 2.1 GHz Band 480 W Doherty Amplifier

The objective of this work was to develop a practical Doherty amplifier with nominally 480 watts of peak power that was capable of linear operation under the UMTS protocol (aided by pre-distortion). Table 1 shows the design targets for the CDPA21480.

A two-way Doherty configuration was chosen, as shown in Figure 1. The input is first divided using a power divider with isolation between its outputs. In this case, we chose a Wilkinson 2-section divider with equal power split. An unequal power split may be preferred for applications with higher peak-to-average signals (WiMAX for example). The two amplifiers (carrier and peaking) are usually quite similar in terms of matching circuits (but not identical), and differ primarily in the gate bias. The carrier amplifier is biased "on" and provides gain at low input levels. The peaking amplifier is biased "off" in its quiescent state, and turns on only after the input signal increases in level. It supplies additional output power (as well as dynamic loading of the

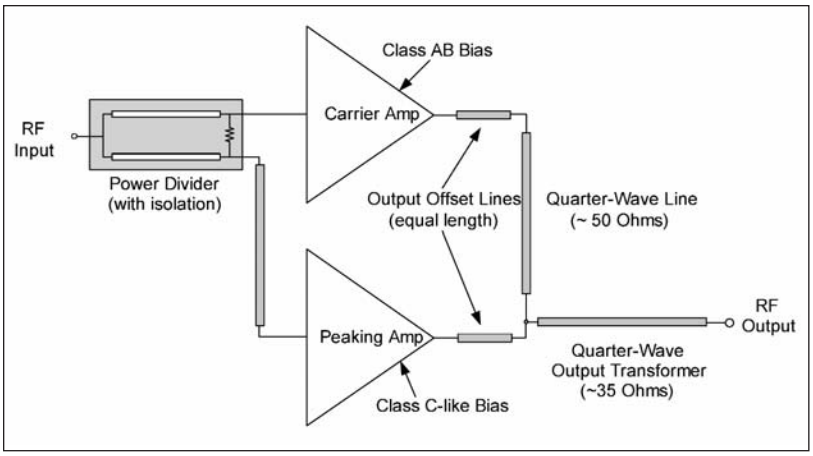

Figure 1 · Two-way Doherty amplifier block diagram.

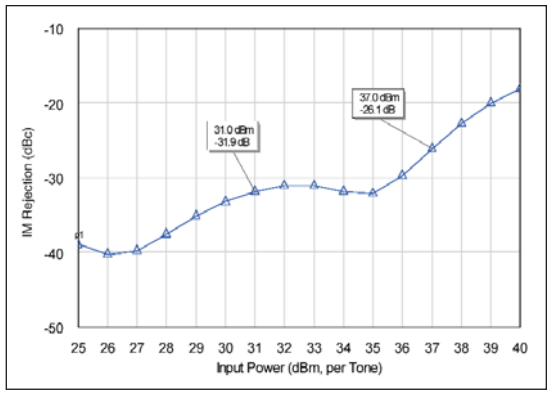

Figure 2 · Typical simulation of Doherty amplifier two-tone intermodulation rejection vs. input power.

carrier amplifier) at high input signal levels. The "turn-on" of the peaking amplifier is dependent on both input power level and gate bias voltage, which in turn influence low RF power efficiency and peak power capability of the total configuration.

The design approach for this relatively high power Doherty design is an extension of that presented previously [3] for a WiMAX amplifier with 1/10 the output level. Of course, the main difference is in the choice of transistors—the Cree CGH21240F GaN HEMT in this case. This device has internal pre-matching (within the transistor package) to simplify input matching required on the PCB. Additionally, this transistor is capable of producing over 240 W output when operated with a +28 V drain supply, with typical gain of 17 dB (Class A/B operation).

The two fundamental considerations for each stage are the bias condition (biased on, or pinched off, and to what degree) and the fundamental and harmonic impedance terminations presented to the transistors. Our approach was to start with a nominal Class J design [4], in which the stand alone stage was optimized in a 50 ohm environment. Then the biases were adjusted for carrier and peaking functions, and the stages were inserted into the Doherty configuration. Next, matching elements of each stage were modified to optimize the Doherty operation. The Doherty output network, specifically including the output offset lines, was also adjusted to maximize critical performance parameters.

One challenging aspect of Doherty amplifier designs is that there are many variables to adjust [5, 6, 7]. These include, for example:

1. Input divider coupling factor (equal in this case).
2. Source impedance for both carrier and peaking amplifiers (including harmonics).
3. Load impedance for both carrier and peaking amplifiers (including harmonics).
4. Output offset line length.
5. Quarter wave input and output line lengths (a quarter wave at the high end of the band in this case).
6. Output transformer impedance.
7. Carrier and peaking amplifier quiescent bias levels.

The initial design approach involved considerable simulation while varying different circuit elements, to synthesize a solution that results in a near-optimum tradeoff of efficiency, linearity, and peak power. Linearity is simulated using two-tone CW signals (as a substitute for the more complex UMTS signal), with a target of achieving intermodulation product suppression better than –25 dBc (–30 dBc for the "hill"). An example of a two-tone IM rejection simulation is shown in Figure 2.

It is particularly instructive to examine the input match conditions as they impact IM rejection, peak power, and efficiency. The Doherty amplifier was partitioned at the transistor gates and a simplified Doherty

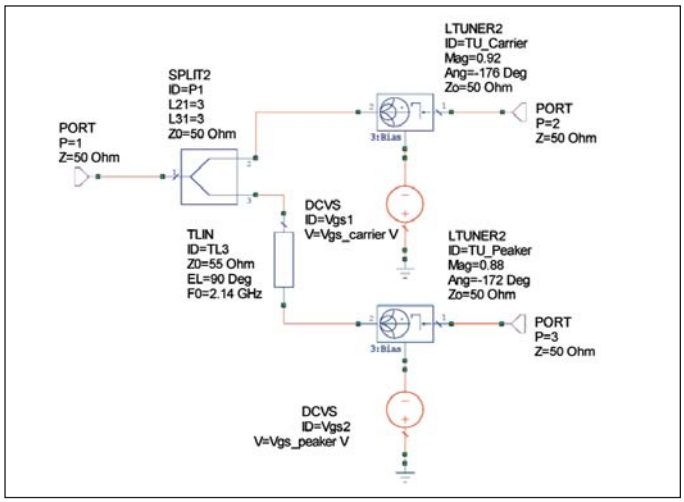

Figure 3 · Test input circuit for source-pull simulations of the Doherty amplifier.

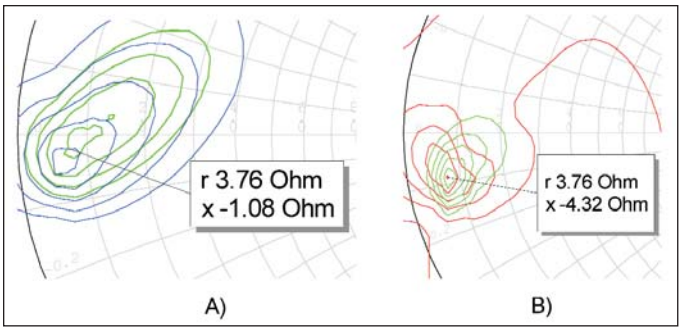

Figure 4 · Source pull of the Doherty peaking amplifier at two input power levels: (a) P_{in} = +37 dBm. Peak power contours (blue, 0.5 dBm step per contour) and IM rejection (green, 1.5 dB per contour); (b) P_{in} = +31 dBm. IM rejection (green, 2 dB per contour) and efficiency (red, 0.5% per contour).

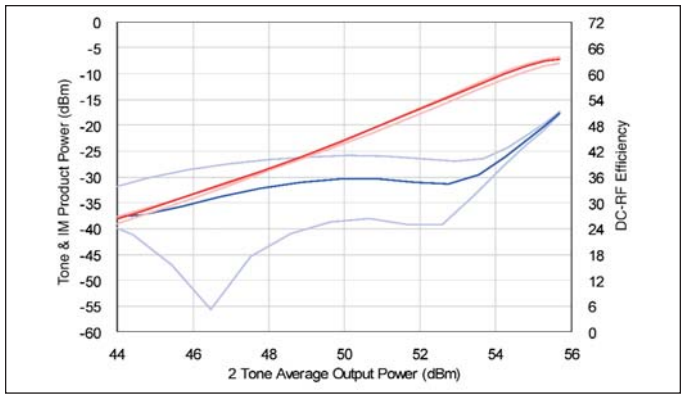

Figure 5 · Simulation of Doherty amplifier two-tone IM rejection and DC-RF efficiency versus output power (while varying the output offset line length ±10 degrees).

input network was substituted, as shown in Figure 3.

This test input schematic allows source-pull of the carrier and peaking amplifier stages in the Doherty configuration. Only one source-pull tuner is activated per simulation. Also, note that the ideal input divider assures isolation between the tuners. Source pull of the peaking amplifier for input levels (31 and 37 dBm) corresponding to peak output level and to back-off hill operation were conducted, with results shown in Figure 4.

The contours of Figure 4 demonstrate the tradeoff in determining "optimum" input match for the peaking amplifier. The contours in Figure 4(a) show peak power and IM rejection for an input power of +37 dBm (per tone). This level corresponds to peak output of the Doherty, and the input impedance for highest power and IM rejection are similar (efficiency is also reasonable, at this high power). The contours in Figure 4(b) are for an input power that is reduced by 6 dB, and corresponds to the back-off hill IM region for the Doherty amplifier. In this case, the contours show an overlapping region for best efficiency and best IM rejection. It is important to note that the optimum impedance for the lower power level (hill region) is quite different than for the peak power case. These contours demonstrate a key aspect of Doherty amplifier design—namely that it is possible to trade off (through peaking amplifier input match) Doherty amplifier peak power for improved efficiency and linearity at backed off power levels (i.e., in a power region that will correspond to the average power of a communications signal with high peak-to-average ratio). Another important variable in this tradeoff process is the gate bias voltage for the peaking amplifier.

A number of simulations while varying the output circuit elements were employed in the synthesis process. The tradeoffs associated with adjusting the output offset line lengths (see Fig. 1) are demonstrated by the simulations of Figure 5. The simulations provide the choice of an offset line length that supports –30 dBc hill IMD levels, while also achieving near optimum efficiency. .

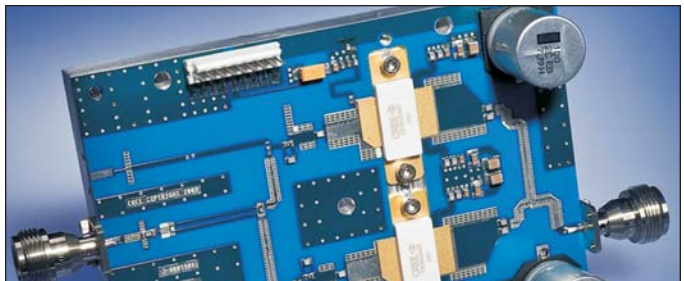

Figure 6 · Photo of the CDPA21480 Doherty amplifier.

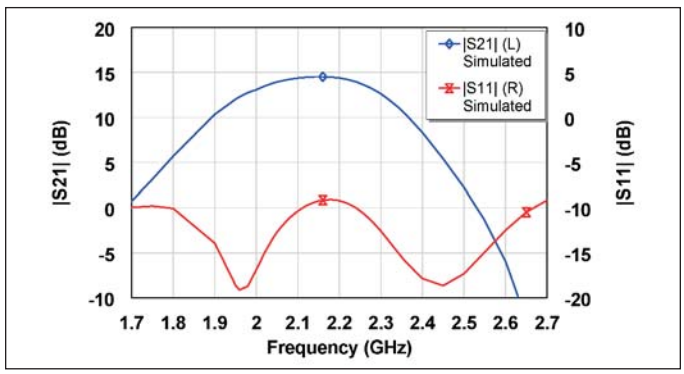

Figure 7 · CDPA21480 simulated small signal response.

The emphasis on minimizing 2-tone IM distortion products while maintaining high efficiency and peak output capability was for the purpose of minimizing distortion under UMTS protocols. The basic assumption is that

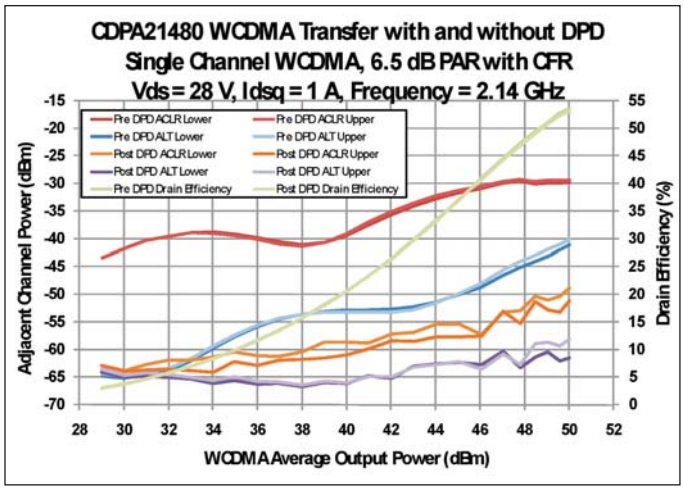

Figure 8 · Measured WCDMA transfer curves.

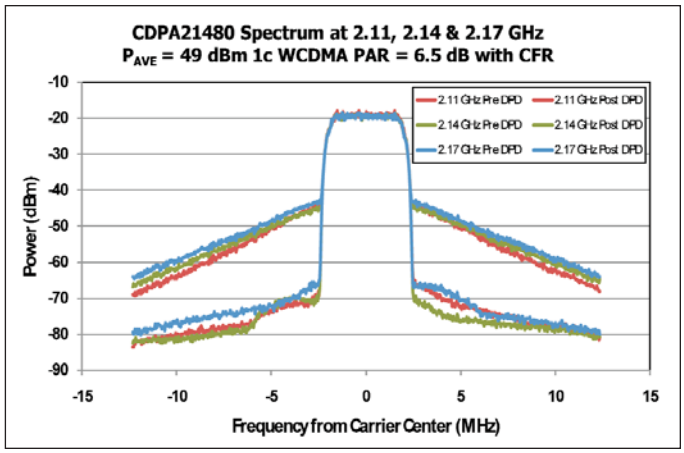

Figure 9 · Single-carrier UMTS output spectrum (with and without predistortion).

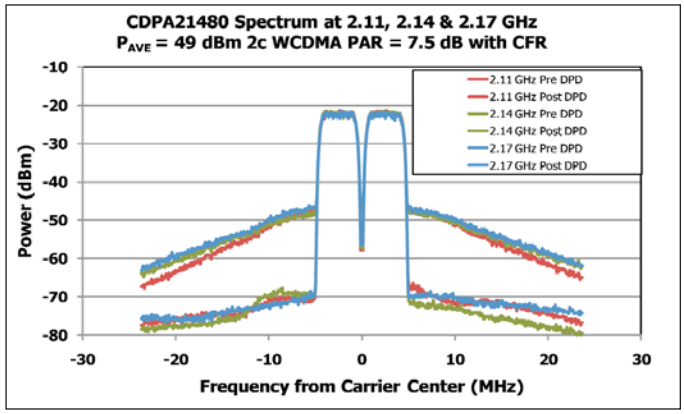

Figure 10 · Two-carrier UMTS output spectrum (with and without predistortion).

achieving a reasonably linear (uncorrected) amplifier will set the stage for highly linear operation when digital predistortion is applied. Our synthesis approach is critically dependent on the availability of good nonlinear transistor models, as is the case for the Cree GaN HEMT devices. These designs were thoroughly vetted using extensive simulations before any physical hardware was fabricated. The simulations were all performed using the AWR Microwave Office nonlinear simulator [8].

Figure 6 shows the assembled version of the UMTS Doherty amplifier (the Cree CDPA21480). Figure 7 shows small signal simulation of the CDPA21480. The amplifier delivers greater than 14 dB power gain across the 2.11-2.17 GHz band. Figure 8 shows single-carrier WCDMA transfer curves with a 6.5 dB peak-to-average ratio (PAR) WCDMA signal (the nearly duplicate curves are for upper and lower adjacent channels). A digital pre-distortion (DPD) system as described in reference [3] was used to correct the linearity. The correction achieved for both single and two-channel WCDMA signals using predistortion is over 20 dB (Fig. 9 and Fig. 10), and well within the applicable standards. At the target 80 W average (single-channel) output power the corrected ACLR1 is better than –50 dBc with 11 dB gain and 50% drain efficiency. Efficiency for the two-channel case exceeds 48% at 80 W average output.

WiMAX 2.35 GHz 480 W Doherty Amplifier

A second Doherty amplifier, the CDPA23480, provides 50 W average power WiMAX performance at 2.35 GHz. This amplifier incorporates an internally matched input CGH25240 transistor designed to provide 240 W peak power from 2.30 to 2.70 GHz. CDPA23480 development followed an identical design path as the CDPA21480 Doherty amplifier. Table 2 shows design targets for the CDPA23480 Doherty amplifier.

Detailed design of this amplifier used Microwave Office software with Cree's large signal transistor model. Large signal simulations allowed for design trade-offs in the simulator to create an optimal design. Due to the higher PAR one trade-off considered was an unbalanced Doherty design [9] to improve linearity further than 6 dB back off. This approach was not pursued since directing more power to the peaker reduced the linear gain of the amplifier. Circuit simulation, tuning and optimization actually pushed the input balance more towards the carrier amplifier to improve gain and linearity. To allow

Parameter	Requirement
Operating Frequency	2.30-2.40 GHz
Modulation Signal	10 MHz wide WiMAX signal
Output Power (average)	50 watts
Drain Efficiency	40%
DPD corrected SEM @ 6.5 MHz offset	–45 dBc

Table 2 · CDPA23480 design goals.

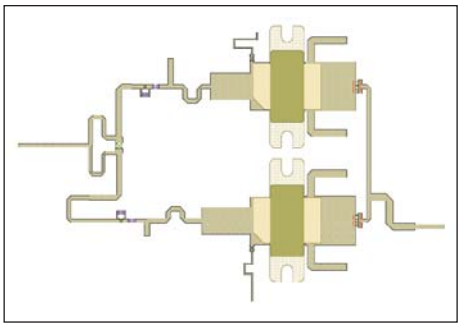

Figure 11 · CDPA23480 AWR layout.

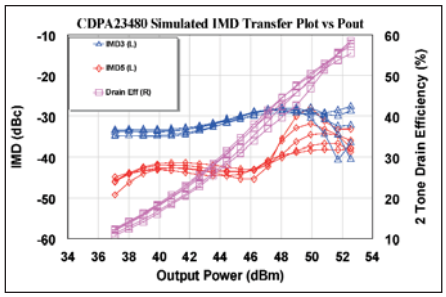

Figure 12 · CDPA23480 simulated linearity results.

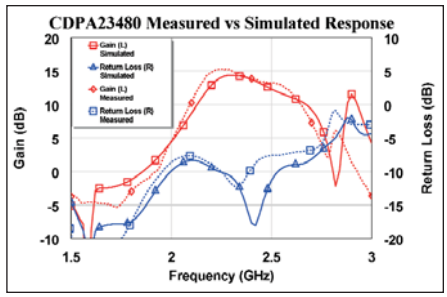

Figure 14 · CDPA23480 simulated vs. measured responses.

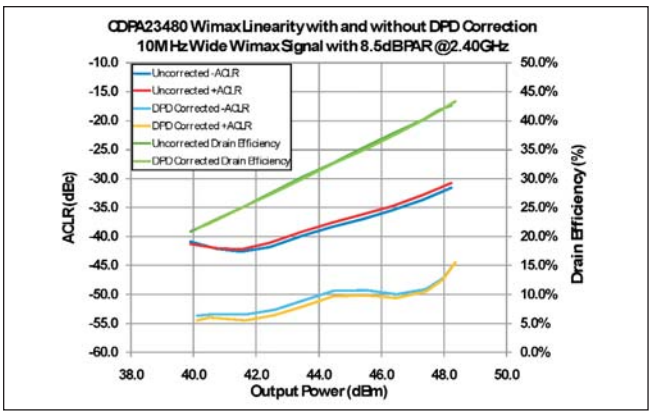

Figure 15 · Measured WiMAX transfer curves.

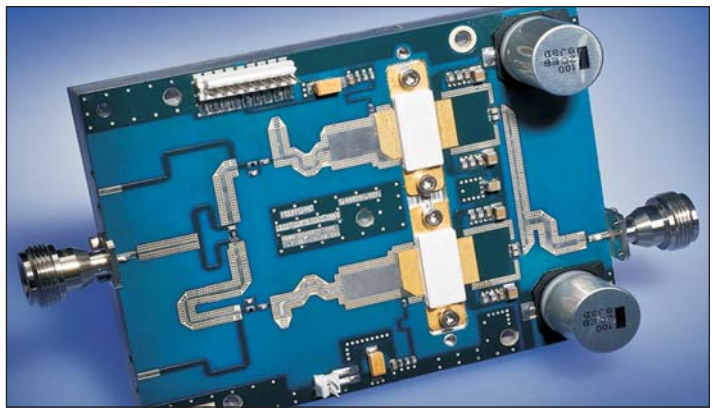

Figure 13 · Photo of the CDPA23480 Doherty amplifier.

design margin, the circuit was designed for 200 MHz bandwidth providing 50 MHz guard bands on each band edge. This wider bandwidth design goal sacrificed some optimal linearity and efficiency to hold uniform performance across the band. Experience shows that a –30 dBc two tone IMD3 design goal provides an amplifier DPD correctable to better than –45 dBc with a 802.16e WiMAX signal. Therefore the design target for simulated two tone IMD3 is –30 dBc. Figure 11 shows the Microwave Office layout of the simulated CDPA23480. Figure 12 shows simulated linearity from 2.25 to 2.45 GHz.

Figure 13 shows the assembled version of the CDPA23480. Figure 14 shows measured small signal data of the CDPA23480 along with simulated results. Small signal correlation is excellent for this amplifier. Figure 15 shows WiMAX transfer curves at 2.40 GHz with and without DPD correction. The 10MHz WiMAX signal corrects to –50 dBc at 50 W (47 dBm) with 39% drain efficiency. Measurements across the frequency band show similar results.

LTE 870 MHz, 120 Watt Amplifier

The GaN HEMT transistors used in the CDPA21480 and 23480 power amplifiers have input pre-matching within the packages. The transistor used in the 900 MHz amplifier, which is the 120-watt peak power CGH09120F, has no internal pre-matching. This allows the device to be used over a wide range of applications at a variety of frequencies. The CGH09120F demonstration amplifier was designed, using Cree's proprietary large-signal model, to have useful performance over 700 to 950 MHz. A summary of the design goals is shown in Table 3.

The power amplifier was realized using a combination of microstrip and lumped element (shunt capacitor) matching. The topology used allows optimum performance to be achieved over frequencies anywhere between 700 and 1600 MHz by adjusting the physical positions and values of the shunt capacitors. The amplifier described here was optimized for best performance around 870 MHz with the intention to exercise the circuit with LTE test signals when available. For the purposes of

Parameter	Requirement
Operating Frequency	700 to 950 MHz
Modulation signal (for testing purposes)	2-carrier W-CDMA with 10 MHz bandwidth and PAR of 7.5 dB
Output Power (average)	20 watts
Drain efficiency	35%
DPD corrected ACLR1	–50 dBc
Operating Voltage	28 volts

Table 3 · CGH09120F demonstration amplifier design goals.

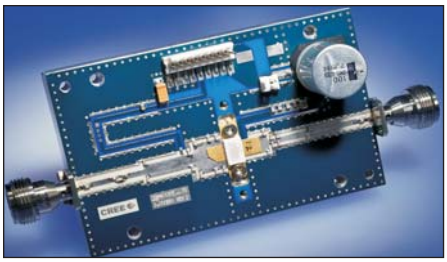

Figure 16 · Photo of the CGH09120 demonstration amplifier.

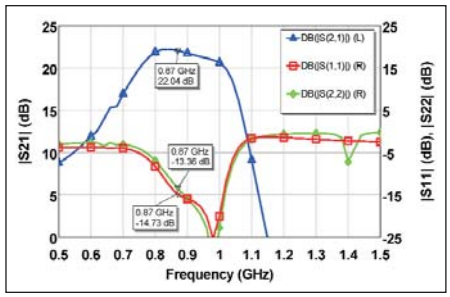

Figure 17 · Simulated small-signal performance of the CGH09120F demonstration PA.

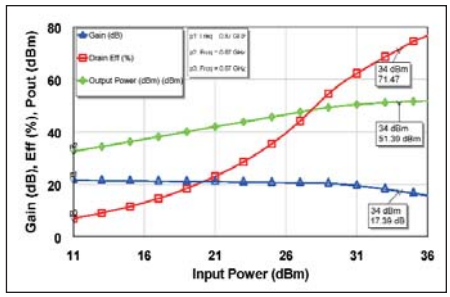

Figure 18 · Simulated large signal performance of the CGH09120F demonstration amplifier.

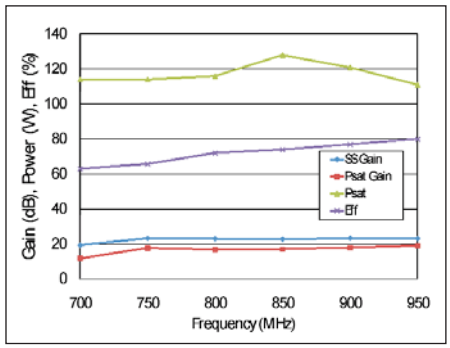

Figure 19 · Measured broadband performance of CGH09120 PA.

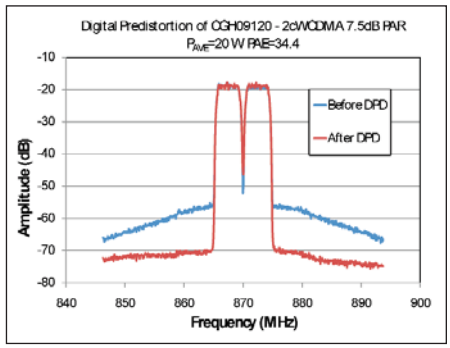

Figure 20 · Pre and post spectral plots of CGH09120F demonstration amplifier.

this article the PA was tested with 2-carrier W-CDMA signals having a total PAR of 7.5 dB and channel bandwidths of 5 MHz.

Figure 16 shows a photograph of the completed single-ended amplifier. The simulated small-signal *S* parameters of the design are shown in Figure 17 and large-signal parameters (gain, output power and drain efficiency) are shown in Figure 18. Measured peak power at 870 MHz was greater than 124 watts with a drain efficiency of 75%. This compares with a simulated peak output power of 134 watts and drain efficiency of 81%. The broadband performance of the amplifier, over the 700 to 950 MHz frequency range is shown in Figure 19. Saturated output power varies from 114 to 128 watts at drain efficiencies of 66 to 80% over 750 to 950 MHz. Measured gain of the amplifier at 20 watts W-CDMA average output power is 21 dB with an accompanying drain efficiency of 35% and native ACLR1 of –36 dBc (in a 5 MHz wide adjacent channel). Figure 20 shows the 2 carrier W-CDMA spectral plots before and after DPD correction. Post DPD ACLR1 is –51 dBc at 20 watts average output power.

Summary and Conclusions

This article has described the design of three power amplifiers for 4G applications. Two Doherty designs employing the new CGH21240F and CGH25240F GaN HEMT transistors show exceptionally high efficiencies while maintaining the ability to be digitally pre-distorted to meet spectral mask requirements. A simpler Class A/B single stage power amplifier design using the new CGH09120F GaN HEMT transistor at 870 MHz has also been demonstrated.

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Ray Pengelly gained his BSc. and MSc. degrees from Southampton University, England in 1969 and 1973, respectively. Since August 1999, Ray has been employed by Cree Inc. Initially, he was the General Manager for Cree Microwave responsible for bringing Cree's wide bandgap transistor technology to the commercial marketplace. On the acquisition of UltraRF in 2001, he became Chief Technical Officer. From September 2005 he has been responsible for new business development of wide bandgap technologies for RF and microwave applications, most recently has been involved with the release of GaN HEMT transistors and ICs for general purpose and telecommunications applications.

Jim Crescenzi received the BS degree at UC Berkeley in 1961 and the MS and PhD degrees at the University of Colorado in 1962 and 1969. He founded Central Coast Microwave Design in 2005, where he provides consulting services primarily for microwave power amplifiers and subsystems. Jim is a Life Fellow of the IEEE for contributions to the development of microwave amplifiers, integrated circuit technology, and miniature receivers for defense applications. He can be reached at jcrescenzi@gmail.com.

Don Farrell received his BSEE from Syracuse University (1984) and MSEE from The Johns Hopkins University (1988). Since 2006 Don has been working at Cree developing high power packaged GaN transistors and circuits. Don is a member of IEEE and has authored numerous magazine articles and papers.

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